What Is Claimed Is:

1. A device for speed negotiation in data transmission, comprising:

a first register for storing an N bit data upon clocking by a first clock;

a second at least one register for storing the N bit data upon clocking by a second clock, the second clock having a clock rate of two times the clock rate of the first clock;

a circuit for receiving the N bit data output from the first register and outputting a first half of the N bit data during a first phase of the first clock and outputting a second half of the N bit data during a second phase of the first clock; and

a multiplexer for receiving as first inputs the output of the circuit and second inputs the output of the second at least one register, wherein the multiplexer outputs the first inputs as a lower speed data and outputs the second inputs as a higher speed data based on a rate select signal.

2. The device of claim 1, further including a parallel to serial converter for receiving the outputs of the multiplexer and providing serialized data output.

3. The device of claim 2, wherein the serialized data is output at a rate of about 2,125 MBAUD.

4. The device of claim 1, wherein the circuit includes N two-to-one multiplexers for receiving at its first inputs the first half of the N-bit data and receiving at its second inputs the second half of the N-bit data.

5. The device of claim 1, wherein each of the first half of the N-bit data is connected to two first inputs of the N two-to-one multiplexers.

6. The device of claim 4, wherein the two to one multiplexer is controlled by an inverted version of the first clock.

7. The device of claim 6, wherein the inverted version of the first clock is delayed to control the multiplexer.

8. The device of claim 1, wherein the second at least one register comprises third and forth registers, the third register for receiving the N bit data, the forth register for receiving the outputs of the third register, the forth register being clocked by an inverted version of the second clock.

9. A method of speed negotiation in a data link, comprising the steps of:

receiving an N bit parallel data at a first low speed path and a second high speed path;

clocking the first path with a first clock, the first clock being a first version of a reference clock;

clocking the second path with a second clock, the second clock being a second version of the reference clock, the second clock is at a higher speed than the first clock;

adjusting the timing of outputting the N bit data from the first path by a factor

equal to (first clock speed) divided by (second clock speed); and

outputting the N bit data from either the first or the second path at the first low speed or the second high speed, respectively.

10. The method of claim 9, further including the step of converting the N bit data output from the first or second paths to provide serial data output.

11. The method of claim 10, wherein the serial data is output at about 2,125 MBAUD.

12. The method of claim 9, wherein the second clock speed is twice the first clock speed.

13. The method of claim 9, wherein the step of adjusting the timing includes dividing the first clock into a first phase clock and a second phase clock and outputting M bits of the N bit data, M being less than N, during the first phase clock, and outputting the N-M bits of the N bit data during the second phase clock.

14. The method of claim 9, wherein the reference clock operates at about 106.25 MHz.

15. The method of claim 9, wherein the step of clocking the second path includes latching the N bit parallel data with the second clock at a first stage and latching

the N bit parallel data at a second stage with an inverted version of the second clock.

16. The method of claim 9, wherein the step of outputting the N bit data includes multiplexing between the first and the second paths, said multiplexing being control by a rate select bit.

17. A device for negotiating speed of a data link, comprising:

means for receiving an N bit parallel data at a first low speed path and a second high speed path;

means for clocking the first path with a first clock, the first clock being a first version of a reference clock;

means for clocking the second path with a second clock, the second clock being a second version of the reference clock, the second clock is at a higher speed than the first clock;

means for adjusting the timing of outputting the N bit data from the first path by a factor equal to (first clock speed) divided by (second clock speed); and

means for outputting the N bit data from either the first or the second path at the first low speed or the second high speed, respectively.

18. The device of claim 17, wherein said means for adjusting includes an N bit two to one multiplexer for receiving at its first inputs the first half of the N bit data and receiving at its second inputs the second half of the N bit data.

19. The device of claim 17, wherein said means for clocking the second path includes a first register for storing the N bit parallel data with the second clock at a first stage and a second register for storing the N bit parallel data at a second stage with an inverted version of the second clock.

20. The device of claim 17, wherein said means for outputting includes a multiplexer for selecting the N bit data from the first or second path under control by a rate select bit.